

AV100 Maintenance Manual

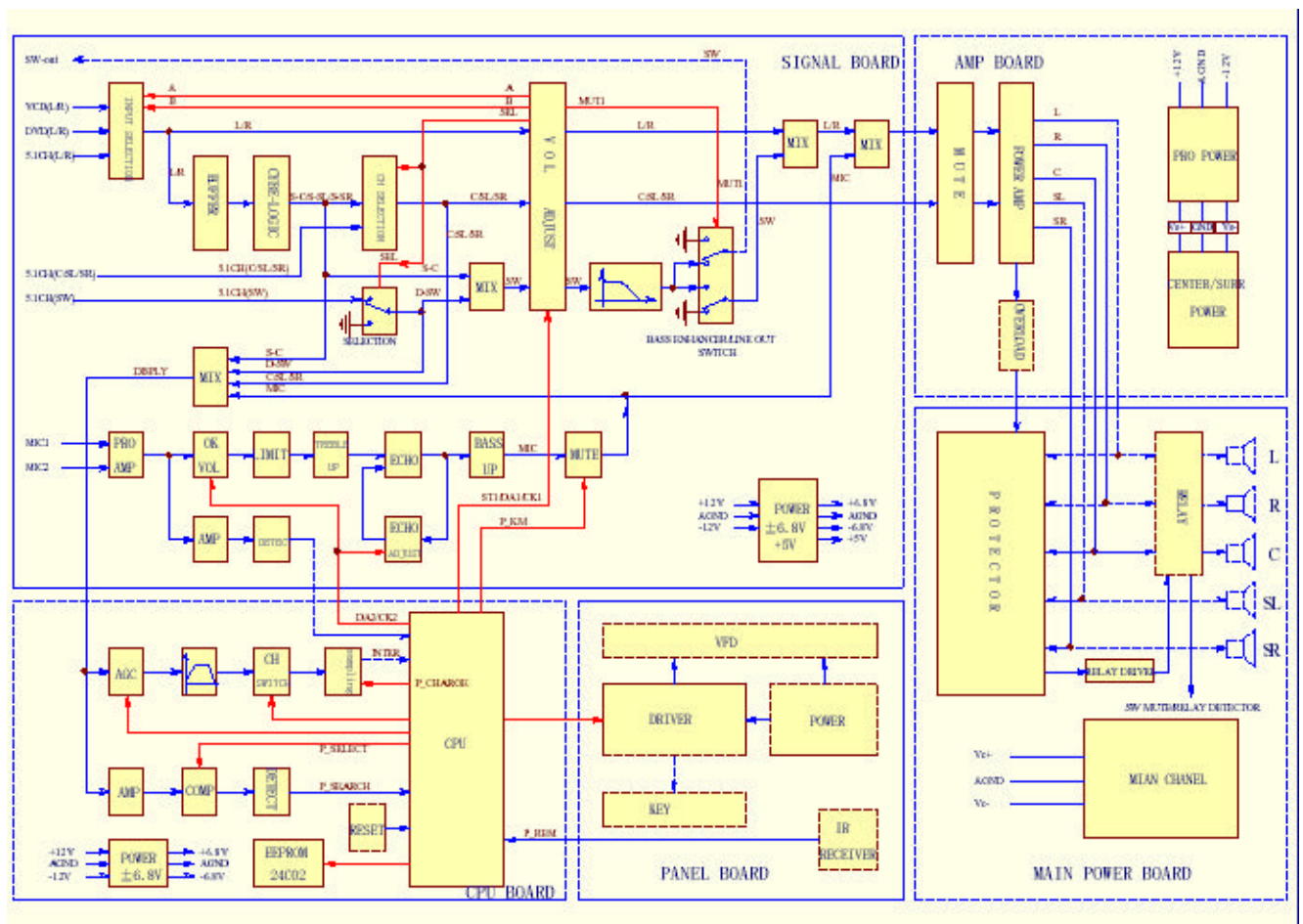
● Precautions:

High voltage inside. Disconnect the power cord from the power supply before servicing!

High voltage components inside. All warnings and instructions on the device shall be followed upon servicing.

Components to be replaced upon servicing shall conform to the specifications. To avoid any danger, do not attempt to modify the parameters of components!

I. Circuit Connection Diagram



II. For the description of operating modes, see User's Manual

Section 1 Device Structure

The entire device of AV100 can be divided into five constituents:

I. Power Supply:

Provide required working electrical power to element circuits including main channel power amplification circuit, central/surround channel amplification circuit, display element circuit, small signal processing circuit and overall control circuit.

II. Signal Processing (including input, cyber logic, bass enhancer and volume control circuit, small signal amplification circuit):

Fulfill selection between input signal sources, cyber logic, bass enhancer, small signal preamplification and independent electronic volume control over channels. “Bass enhancer” function is unprecedentedly added to AV100.

III. CPU Control

Being the control and processing center of the entire device, it consists of CPU, panel control and software recognition circuit, providing users with a “man-machine conversation” environment, so as to fulfill process control, protection function control and frequency spectrum display.

IV. Microphone Circuit

It consists of small signal preamplifier circuit and echo processing circuit, and will finally be sent into the preamplifier of main channel and main channel for mixed amplification

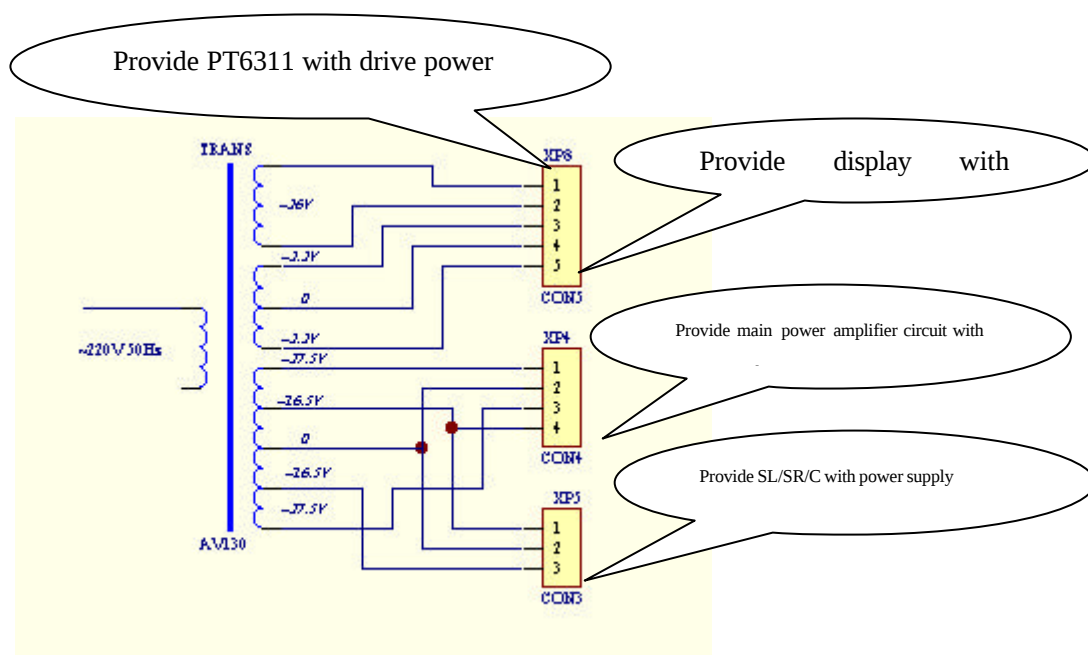
V. Power Amplifier and Protection Circuit

Conduct post power amplification for small signal. Meanwhile, conduct automatic protection for power amplifier circuit and speakers.

Section 2 Power Circuit

It provides working voltages required by circuits of the different units. See different levels of transformer outputs below:

- I. The DC power supply of $\pm 32V$ is obtained via the rectification and filtration of two sets of AC 26.5V outputted from the transformer at first sublevel by four IN5404s



and two big electrolytic capacitors (4700uF/35V), providing power to left and right

channels.

- II. The power supply of $\pm 22\text{V}$ is obtained via the rectification and filtration of two sets of AC 16V voltages outputted from the transformer at second sublevel by four IN5404s and two electrolytic capacitors (2200uF/25V), providing power to SL/SR/C channels, and also to other IC and operational amplifiers after voltage stabilizing via voltage stabilizing tubes L7812 and L7912;

AV100 is provided with standby function, using CPU software program to mute all channels in standby mode.

Section 3 Input, Cyber Logic and Volume Control Circuit

The cyber logic function of AV100 is realized by C/SR/SL and SW channel signals obtained after processing signals extracted on L/R channel by using low pass filter and band pass filter. This circuit uses several electronic analogue switches to fulfill switching between different modes (See Figure II for signal flow).

I. Input selection and mode switching circuit

AV100 has two sets of analogue audio source input modes and a set of 5.1 input jack. The switching between them is realized by using electronic switch. Two types of electronic switch IC are used in the circuit: CD4052 (2-channel 4-option electronic analogue switch) and CD4053 (3-channel 2-option electronic analogue switch). Their truth tables are as follows:

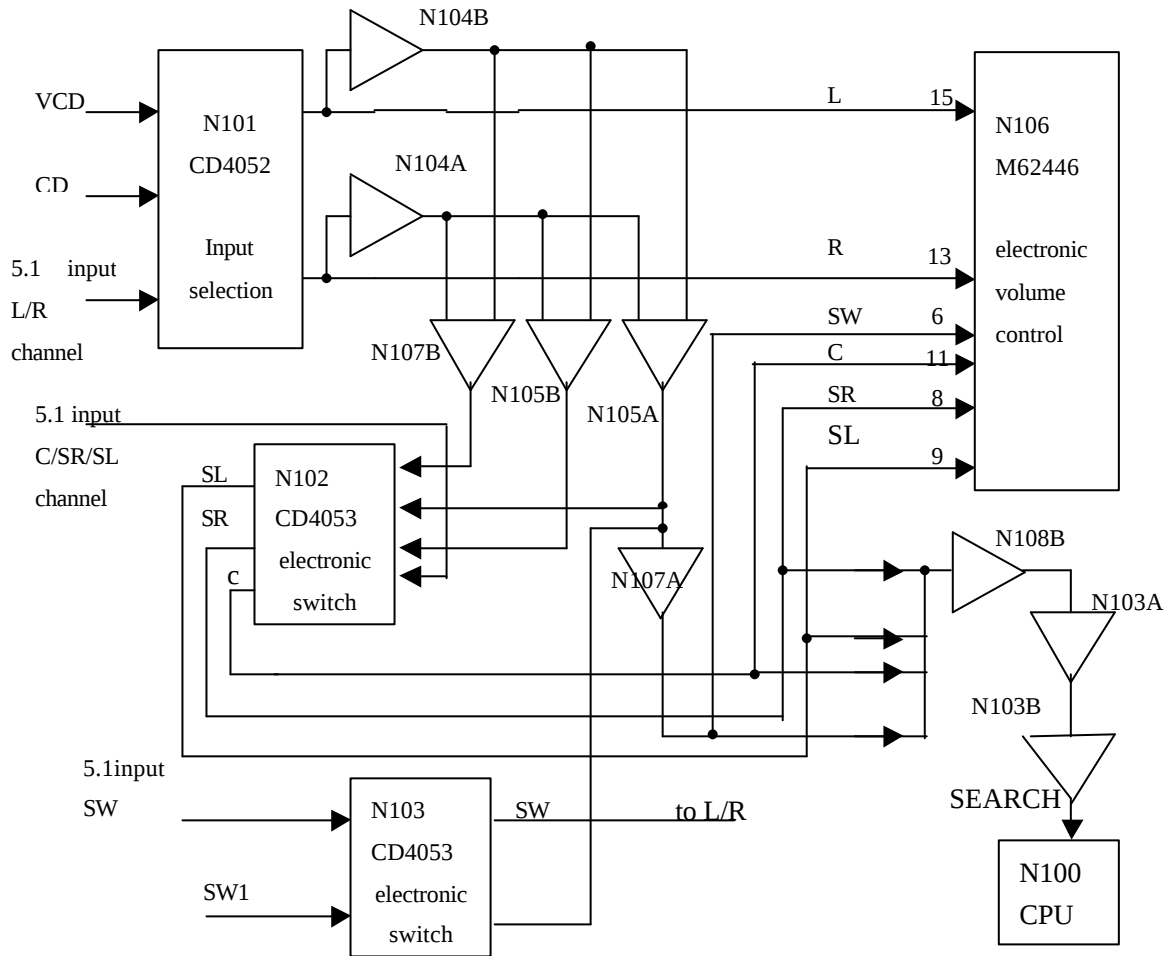
CD4052		Truth		
	X0	X1	X2	X3
A	0	1	0	1
B	0	0	1	1

CD4053		Truth			
A	X	B	Y	C	Z
0	X0	0	Y0	0	Z0
1	X1	1	Y1	1	Z1

In this circuit, there are another two important control signals, i.e. SEL and MUT1. When SEL is of high level, the circuit is in external “5.1 channel” input mode; when SEL is of low level, the circuit is in “Cyber Logic” mode; when MUT1 is of high level, “Bass enhancer” function will be enabled; when SEL and MUT1 are all of low level, the circuit is in standard sound field processing mode. Here is a detailed analysis:

When pressing “input” button, IC SC0791 on the control panel will recognize its code and send an execution request signal to CPU. Then the 32nd pin of CPU (N100) will return a data signal to M62446. According to the “input” button status, the 1st/2nd/3rd/4th pin of M62446 sends corresponding high/low levels, the combination of which will enable electronic switch to circularly select between VCD? DVD? 5.1CH. Now there are mainly two statuses: two analogue input statuses (VCD/DVD) and 5.1CH input status. Their respective signal flows are as follows:

1. 5.1CH input status: When A/B/SEL control lines of M62446 are of high level, L/R channel signal of 5.1 input end is outputted from pin 3,13 of N101 and sent to IC N106 for functional adjustments of channel volume, sound field balance, etc.; meanwhile, the 4th pin of N106 outputs a high level to pin 9,10,11 of electronic switch N102 (i.e. SEL control signal), and C, SR, SL signal on



(Fig. 2)

5.1 input terminal is respectively sent from pin 14, 15, 4 output of N410 to IC N106 for independent volume control. SW channel signal on 5.1 input terminal is sent to pin 3 of IC N103, while pin 9 (SEL) is of high level, and SW signal is sent from pin 4 output to IC N106 for volume control. Now the six channel signals of 5.1 input terminal are all sent to electronic volume control IC for independent volume control and then outputted post pole circuit. The signal source of the device is in 5.1 channel input mode.

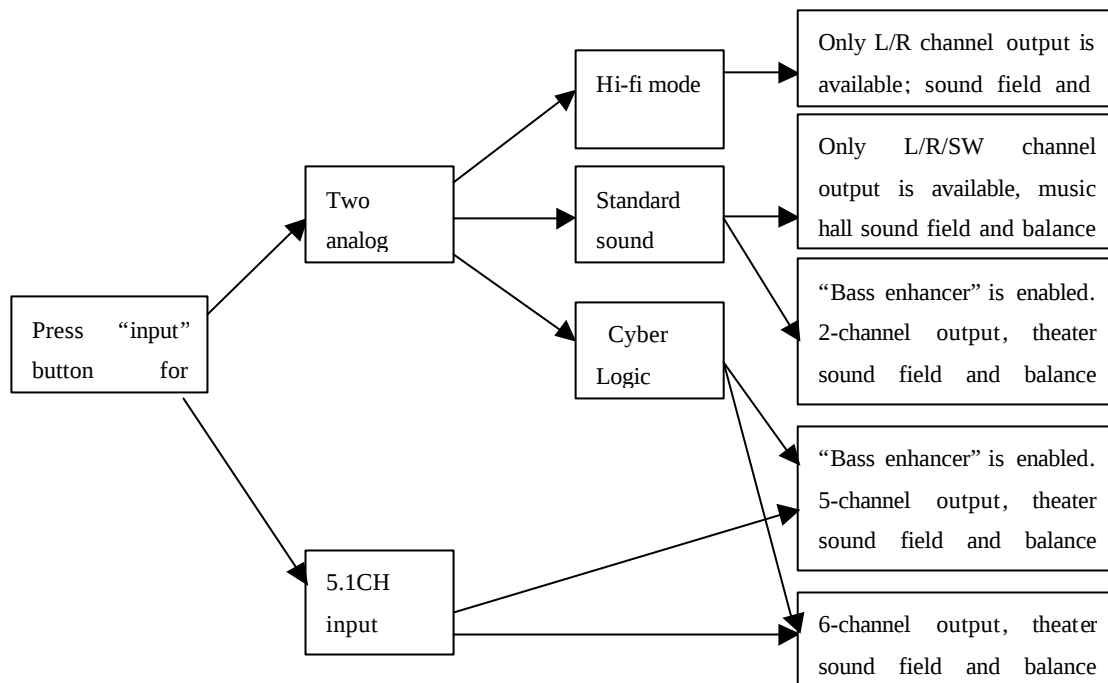
2. Two analog input modes: Press the input button on the panel to select from two analogue input modes of VCD and DVD as signal source. The selection is also realized via data signal sent from pin 32 of CPU N100 using pin 1, 2, 4 of M62446 to send three control levels of A, B and SEL to pin 9, 10 of electronic switch N101 (pin 9, 10, 11 of N102). L/R channel signal is subject to volume/tone control and sound field mode directly via M62446 from pin 3, 13 output. AV100 has three processing modes for signals: hi-fi, cyber logic and standard sound field. Their respective signal flows are as follows:

- 1) Standard sound field processing mode: L/R channel signals outputted from N101 are directly added to IC N106 for electronic main volume control. Meanwhile, SW signal obtained by amplifying a signal from L/R channel via N104 voltage followed by N107A two-level low pass filtering is added to pin 6 of electronic volume M62446 for electronic volume control. MUT1 is of low level; now the device is in 2-channel input and 3-channel output mode. When MUT1 is of high level, "Bass enhancer" function is enabled. Now the device is in 2-channel input and

2-channel output mode.

- 2) Hi-fi processing mode: (mainly for VCD/DVD input mode): The signal flow is same as that of stand sound field mode, but under the control of CPU, electronic volume control IC N106 closes other channels and disables sound field processing and balance control. Therefore, SW/C/SL/SR channel has no output and the device is in 2-channel input and 2-channel output mode.
- 3) Cyber logic mode: L/R channel signals outputted from N101 are directly sent to IC N106 for electronic main volume control. Meanwhile, two ways of surround channel signals are obtained by adding and subtracting using N105 (4558) after amplifying two ways of signals from L/R channel via N104, central channel signal is obtained through N105A, and SW signal source is obtained through N107A inverse amplification, and is inputted to pin 6 of M62446 (Note: SW signal of cyber logic is obtained through the output terminal of M62446 and then through a 2nd order low-pass filter); now pin 9/10/11 (SEL) is of low level and SW signal source is directly sent to pin 6 of M62446 for electronic volume control. MUT1 is of low level, and now the device is in 2-channel input and 6-channel output mode; when MUT1 is of high level, “Bass enhancer” function is enabled and now the device is in 2-channel input and 5-channel output mode.

The relations between switching between audio sources of input circuit and sound processing modes are as follows.



II. Volume control, sound field processing and EQ control circuit

Channel signals are finally sent into N106 to fulfill independent volume control, EQ control and different sound field mode processing, etc.

Sound field processing and EQ control circuit is mainly for the processing of L, R main channel signals. As seen from the schematic diagram, L, R channel signals are sent to pin 13, 15 of N106. When the device is in hi-fi mode, CPU software program will control M62446 and mute other channels, and volume control is only available for L, R channel, and only pin 31, 32 has signal output, while the device is in 2-channel output mode; when the sound field mode of the device is not in hi-fi mode, independent volume control of each channel and sound field processing or EQ adjustment of L, R main channel are available. Finally, signals of different channels will be

outputted from pin 31, 32, 33, 34, 35, 36 of N106. SW channel signal outputted from pin 36 will be sent into pin 1, 12 of N103 after passing an active low pass filter. The level signal of MUT1 will decide whether outputting it to an active speaker for amplification by SW output terminal or sending it to main channel to enable “bass enhancer” function. Other channel signals will be sent into power amplifier circuit for post power amplification. L, R channel signal will pass two-level mixed amplification (superpose subwoofer or karaoke signal onto L/R channel).

“Bass enhancer” function:

”Bass enhancer” function is to send subwoofer elements to left and right channels respectively so as to enhance the bass effect on main channel. At this time subwoofer speaker has no output and an active subwoofer speaker can be saved; but this will increase the power load on main channel, placing a high requirement on post amplifier. Primarily comparing with standard sound field, cyber logic and 5.1 input sound field mode, its operating principle is as follows:

When the device is in any of the three modes and “Bass enhancer” function is enabled, CPU will send a data signal to IC M62446, pin 32 of which will send a high level signal to pin 10, 11 of N103, so that pin 14 of N103 will be grounded (signal outputted to SW is closed), and SW signal will be outputted from pin 15 of N103 to the reverse phase of N109A/N109B for mixed amplification with L/R channel, followed by post amplification in main channel power amplifier circuit after N110 amplification. For the three modes of “Bass enhancer”, gradual volume increase is done by IC M62446 and each time an increase of over 3dB over the previous grade is done.

III. Input signal detection, search and spectrum sampling circuit

1. Input signal detection, search circuit: After synthesizing and gating, input signals are mixed by sample resistances R133, R134, R135, R136, R195 connected to the output terminals of N102 and N103 and then amplified at the inverted input terminal of N108A. Then input signals are level amplified and clipped by N103A on CPU board, and then sent into voltage comparator made up of N103B. The output terminal of N103B is connected to pin 16 of CPU through a triode (switch tube). When the output terminal of N103B outputs a high level, VD103 is in inverse cutoff state and the E pole of switch tube V101 is of high level. Therefore, the switch tube is in conducting state. Then through voltage regulation by N103B, an obtained high level of about +5V returns to CPU, indicating no signal input is detected; when the output terminal of N103B outputs a low level, VD103 is in positive conducting state, and the E pole of switch tube V101 is of low level. Therefore, the switch tube is in cutoff state. Through VD101, a low level returns to CPU, indicating there is signal input; when it is of low level, CPU stops searching. See details below:

- 1) After startup, pin 32 outputs a data signal to M62446 under the control of CPU internal program, and then M62446 sends high/low level to scan each input port of N101, N102, N103. When none of these input ports has signal input, it will automatically stop in VCD mode (display the previous off state “connect to ***”). When one input port has signal input, and this signal is greater than about 15mV, AC signals will be present on channels of N101. This AC part, after N104 amplification and amplification on N105A, N108B and N103A on CPU board and level clipping, is compared with pin 1 of N103B and then a high/low level of power supply is obtained. Now the positive voltage is about 0.35V. When this DC voltage exceeds 0.35V, the output terminal of N103B outputs low level close to negative supply voltage, so switch tube V101 (S9014) cuts off. Through VD102 and R109, a low level returns to pin 16 of CPU, indicating CPU has searched signal, the CPU locks search level on this port with signal input via controlling IC M62446 and enters into normal playback.
- 2) When “search” button on remote control is pressed, optical signal received by remote control

receiver is converted into electric signal, and then pin 14 of CPU sends a high level to put V102 into conducting state. Search is done in the same way as procedure one.

- 3) At the same time, AV100 has “auto mute” function: When input signal is less than about 1mV, CPU will put the device into “auto mute” mode; the signal control flowchart is as follows: When CPU “finds” signal, pin 14 of CPU will immediately shift into low level, so that V102 is in cutoff mode. After +12V is voltage divided by R113 (180K) and R114 (100O), a voltage of about 1mV is obtained on the positive end of N103B. Therefore, external signal, after sampling and amplification, is compared with this voltage. If it is smaller than this voltage, CPU turns the device into “auto mute” mode; or when CPU has not found signal, the device will also be turned into “auto mute” mode by comparing the voltage division between the reverse end and R1113/R114.

2. Spectrum sampling and amplification circuit: Signal channels have sample resistances R133, R134, R135, R136, R195 respectively. After signals are mixed by them and sent to be amplified by N108B, spectrum analysis signal source (DISPLAY) is obtained and sent to band pass filter circuit of CPU board.

Section 4 Overall Control Circuit

The overall control circuit of AV100 is divided into three parts, i.e. CPU control circuit, protection circuit, panel control; display drive circuit and spectrum analysis circuit.

I. CPU circuit

N100 (SM89C58) is the overall CPU, being the processing and control center of the device that outputs control commands to controlled circuits and fulfills control functions. It adopts +5V power supply and pin 40 is the power supply pin. 12M crystal oscillator connected to pin 18/19 provides working clock frequency. Pin 9 is its reset pin. Upon startup, +5V is added to the positive pole of C106 via R100. Since that E pole voltage of triode is greater than B pole voltage, V100 turns on and +5V voltage charges up C105. When the theoretical high level (over 3.6V) is reached, CPU begins to reset, its resetting time being the charging time of +5V power supply against C106. When the charging voltage on C106 is greater than 4.3V, V100 begins to cut off, and pin 9 of N100 returns to low-level state. In this way, CPU fulfills resetting and the system starts up normally. This reset circuit is in the form of high level resetting, maintaining low level. Refer other control commands to circuit diagram.

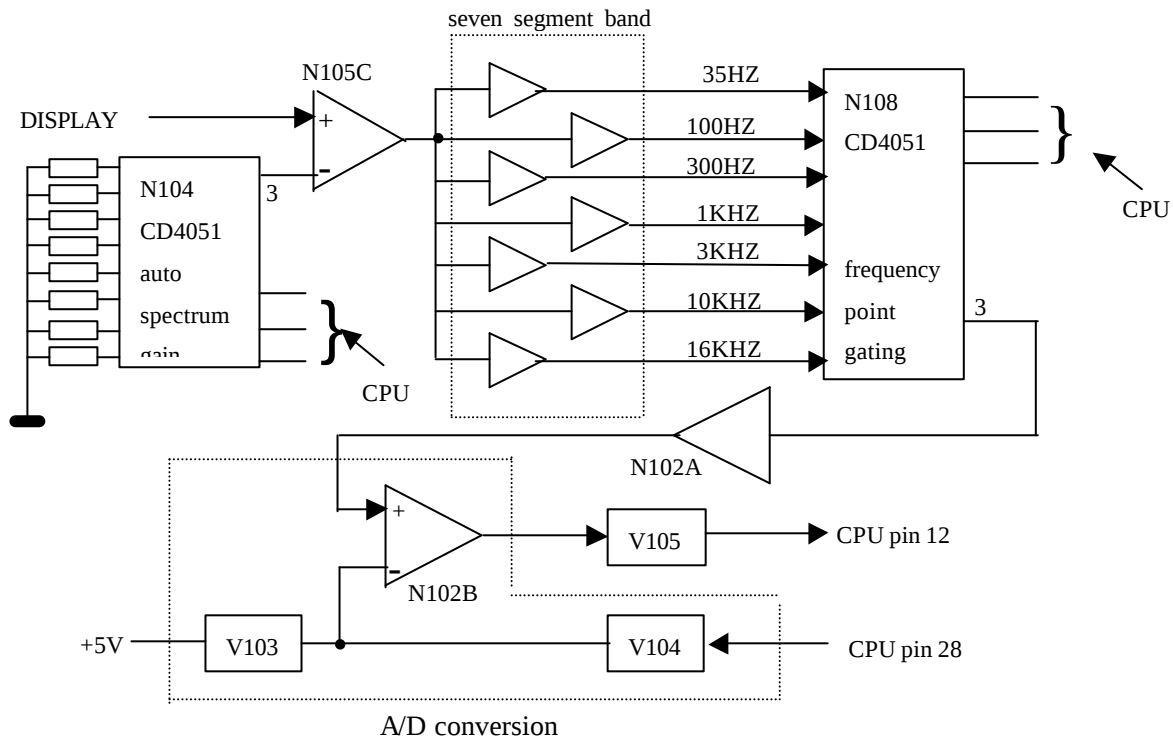
The startup picture, Chinese characters displayed during operation and other static information are saved in the built-in static memory of CPU. N101 is a status register that records working statuses upon shutdown and recalls these statuses upon the next startup (after more than 3 seconds from the previous shutdown), avoiding readjustment by the user. User defined sound field mode is also saved in it and can be recalled when required.

II. Panel control and display circuit

The panel control and display circuit of AV100 uses dedicated IC 101 (PT6311). Its pin 10/11/12/13 are externally connected to scan button matrix. After the overall control command from the user is received, two-way outputs are available: one way is sent to the display to show its working status and another way is transmitted to CPU via pin 5/6/8/9 for requesting the execution and fulfillment of corresponding control function.

N102 is a remote control receiver that transforms infrared remote control signal into electric signal and then send it to pin 13 of CPU to fulfill remote control function.

III. Spectrum analysis circuit (see flowchart diagram below):



Spectrum analysis circuit can be divided into three parts:

1. Automatic spectrum gain adjustment circuit: To avoid ultra low width spectrum display when the input signal is too weak or full screen display when the input signal is too strong, AV100, as its predecessors, provides automatic spectrum gain adjustment circuit, using a single channel select-1-from-8 electronic analog switch N104 (CD4051), the truth table of which is as follows. Its working principle is, generally, to change the value of the reverse ground resistance of operational amplifier N104 by switch selection so as to change the gain times of operational amplifier. Let us see the specific working process of the whole circuit.

The abovementioned spectrum analysis signal source (DISPLAY) is sent into the in-phase input

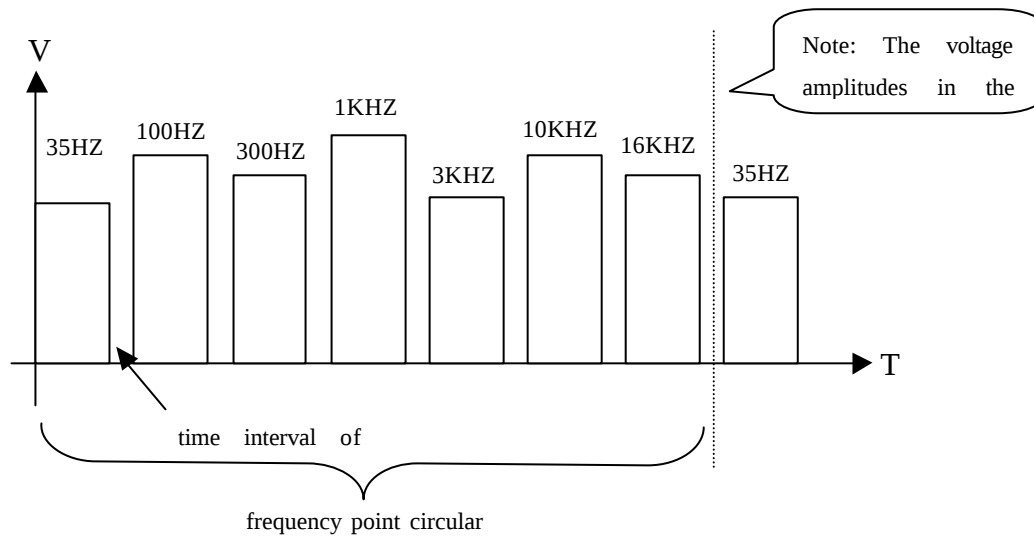
	CD4051				Truth			
	X0	X1	X2	X3	X4	X5	X6	X7
A	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1

terminal of operational amplifier N105C for amplification. The amplification times is dependent on the value of the resistance connected to the reverse end via N104 electronic switch. When the input signal has a rather high amplitude, CPU will automatically control pin 9/10/11 to gate higher valued resistance to increase ground resistance value and reduce simplification times to reduce the gain; when the input signal amplitude is rather smaller, CPU will automatically reduce the value of ground resistance and increase amplification times.

2. Frequency point gating circuit: Signals amplified via N417B and coupled by C114 are sent into

7 band pass filters made up of operational amplifiers. By setting its feedback capacitance its corresponding frequency band range can be determined. The frequency values marked on their output points are the central frequency points of this frequency band. A half-wave rectification circuit is connected to the output terminal of each band pass filter to rectify amplified AC signal into DC voltage. This circuit is mainly for the realization of frequency point sampling and can present the amplitude of each frequency point in a complete sound signal through DC voltage. If low frequency prevails in sound signal, DC voltage on 10K/16K band pass filter will be higher. The output terminal of these seven band pass filters are connected to the seven input terminals of electronic switch N108 (CD4051) and this electronic switch can realize rapid gating between frequency points via control commands sent by CPU (refer to the above truth table). A series of voltage values representing frequency point signal amplitudes will be outputted on the output terminal of pin 3 of N108.

3. A/D conversion, display output circuit (discussed in two cases)



1. When there is no signal input (i.e. no detect-in signal), CPU pin 28 will send a high level to V104 C pole to put it into conducting state. And since E pole and B pole of V103 are provided with +5V power supply and a biasing circuit made up of VD115 and VD116, maintaining V103 in conducting state, so the circuit will not charge up C137, the positive end of N102B is of low voltage and the reverse end of N102B obtains voltage division of R169 and R172, and so N102B will output a low level, i.e., triode V105 cuts off, and V105's C pole will send a high level to pin CPU's pin 12, informing CPU no to conduct AD conversion (CPU's pin 6/7/8 does not act, maintaining at high level.)

2. When the device detects signal (i.e. when a DC voltage representing 35HZ signal amplitude is present on the reverse end of N102B), CPU's pin 28 will immediately be converted into low level, and meanwhile, +5V provides V103 with conducting condition and outputs high level from V103's C pole and charges up C137, the positive end (the inphase end of N102B) voltage of which will increase gradually. When the voltage of reverse end is reached, the comparator inverts, and N102B output is close to the high level of positive supply voltage. Once the comparator inverts, CPU will immediately terminates 35HZ level gating and switches to the next frequency point 100HZ. During the instant of their switching, an instant high level outputted from CPU's pin 1 gates V104 and discharges the voltage capacity on C137, allowing the inphase end of N102B to resume 100HZ charging from 0 level. When 100HZ charging is complete, it will turn into the next charging and discharging process for the next frequency point. Such processes will be circulated under CPU control. The charging time from 0 level to the occurrence of output inversion represents the signal

amplitude of the current frequency point—the greater the amplitude is and the longer the time is, the higher the amplitude displayed on the screen will be; the smaller the amplitude is and the shorter the time is, the lower the amplitude displayed on the screen will be. As known from the above circuit working process, a series of analog DC levels originally with specific voltage values become a series of digital pulses only with two states of 0 and 1 presenting the original information by its time duration. And so the conversion of analog/digital (A/D) is done. Digital pulses outputted from the output terminal of N102B, inverted by V105, are sent to pin 12 of the CPU, which process and output them to panel display IC N101 for dynamic spectrum display on the display. Originally frequency points are displayed in order, but what we see on the display is a working process with the whole spectrum displayed simultaneously since the abovementioned circulating process is so rapid.

Section 5 Microphone Circuit

Microphone circuit can be divided into two parts: preprocessing and echo processing.

I. Preprocessing circuit: to fulfill volume control, amplification and modifying. The flow diagram is as follows:

Two-line MIC signals inputted by two-line microphone jacks, after preamplification, are divided into two lines, one is sent to the reverse end of N111B for inverse amplification followed by rectification and filtration via VD103/R208/C206 producing a high level, so that V103 is turned on, and V103's C pole returns a low level to CPU, indicating that MIC signal is found; the other, after coupling by C207, is inputted into N112 M62429 followed by volume control by IC, and mixed and amplified with high frequency signals obtained from the high frequency boost network made up of R219, R220, C233 and C234, and then send to echo and delay IC PT2399, the IC of which fulfills the echo and delay of karaoke.

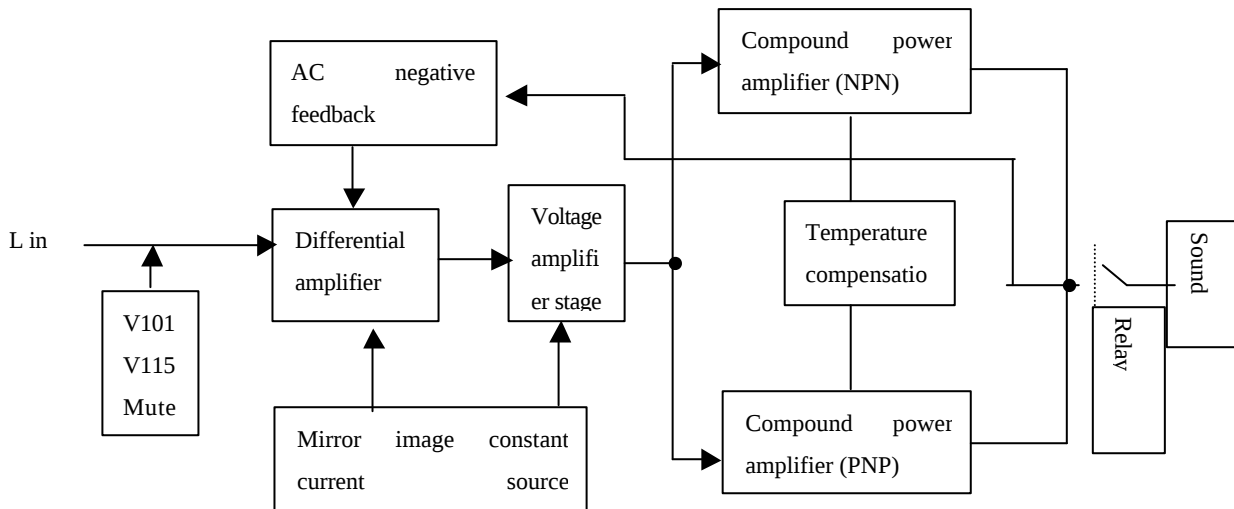
II. Echo processing: After being mixed and amplified by N111C and coupled by C213 and R224, signals are inputted into pin 16 of echo processing IC N113 (PT2399), in the inside of which signals are subject to low pass amplification and digital delay processing, and then outputted from pin 14. Pin 6 is externally connected to echo delay adjustment resistance. Signals outputted from pin 14, after being coupled by R230, C223, R235 and C209, are inputted into pin 1 of M62429 for volume increase, and then pin 2 outputs and feed backs to N113's pin 16; and finally PT2399's pin 15 outputs them, C217 couples them and inputs them to pin 12 of N111D, and then they are mixed and amplified with the low frequency boosted by a low frequency boost network, and send to the reverse end of N110A and N110B, where they are superposed with L/R main channel and send to power amplifier circuit for power amplification. And besides, karaoke is provided with auto mute function against microphone insertion impact sound. This control process is as follows (in two states):

1. When the device is reset, CPU's pin 25 will immediately outputs a high level to conduce V100 via R193, so as to conduce V101, making short circuit to earthing of MIC signals, so as to mute karaoke noise signals;
2. When inserting a microphone and signals are detected by CPU's pin 5; CPU's pin 25 will returns a low level. Due to charging and discharging of C169, the cutoff of V100 and V101 requires a waiting time, so the impact sound and mechanical noise can be removed effectively.

Section 6 Power Amplifier and Protection Circuit

The description and block diagram of the working principle of main power amplifier circuit are as follows:

I. L/R channel power amplifier circuit: The L/R main power amplifier circuit of AV100 adopts



discrete components. Its circuitry principle is as follows (taking L channel as example).

When being outputted by electronic volume control circuit, L channel signal is sent to power amplifier stage. Mute circuit is provided on the input terminal: When the mute button on remote control is pressed, a “mute” signal is obtained after photovoltaic conversion by remote control receiver and returned to CPU, so that CPU’s pin 35/36 send a high level “mute” command, allowing positive biased conduction of V115 (main channel) and V130 (central channel), and V101 is successively conduced, fulfilling mute control. The mute control of surround channel is fulfilled by directly adding high level to LM4731’s pin 6/11.

L channel signal, after being coupled by R103 and C101, is sent to the differential amplifier circuit with double ended input and single ended output consisting of B pole of differential amplifier stage, V102 and V103. Audio signal is outputted from C pole of V102 to B pole of voltage amplifier stage V105, and outputted to compound power amplifier stage after voltage amplification. V104, V107, VD102 and VD103 constitute mirror image constant current source circuit. VD102 and VD103 provide V104 and V106 with constant base current. The emitter resistance of V104 determines the working current of differential amplifier stage and the emitter resistance of V107 determines the working current of voltage amplifier stage. V108, V109 and V112 constitute the upper tube (NPN) of the compound power amplifier. V108 and V109 are connected in parallel, acting as a medium power triode (to increase output power), and compounded with V112 to constitute NPN type multiunit tube (to increase amplification times). V110, V111 and V113 constitute the lower tube (PNP) of the compound power amplifier. Its circuit structure is same as that of the upper tube but its type after compounding is PNP. Temperature compensation tube V106 plays two roles in the circuit: First it is the base bias of upper and lower geminate transistors, and its working status determines the static working current of the compound power amplifier, that is to say, we can set the static working point of the compound power amplifier stage by adjusting the conduction of V106 and the usual way is to change the base resistance of V107; it can also automatically adjust the working status of compound power amplifier stage upon temperature rise. The adjustment process is as follows:

Total current of output stage = working current + leakage current

When the temperature rises, the increase of leakage current causes drift of static working points
(disadvantageous)

Meanwhile, the leakage current of V106 increases and U_{ce} decreases,

reducing the bias current, changing working status and working current of post pole. The total current is controlled within a certain range.

Voltage negative feedback is introduced into the power amplification circuit of AV100 and consists of R121, R109 and C105, the parameters of which determine the major closed-loop gain times of the whole power amplifier. The formula is: gain times = $1 + R121 \div R109$. AV100 uses direct output and R111 and C116 connected to the output terminal constitute Zobel network, which can prevent high frequency self-excitation caused by AC inductive reactance of loudspeaker voice coil.

II. C/SR/SL power amplifier circuit: Compared with its predecessors, these three channels of AV100 use dedicated power amplifiers LM4731 and IC LM1875. For LM4731, it has totally 15 pins. Pins 2/4/15 are its positive and negative power supply pins, and pins 7/8/12/13 are its in-phase and reverse input terminals. Meanwhile, it uses independent positive power supply for two channels. The rated power of each channel of this power IC can reach 25W. The high level automatically “mutes” upon startup. Pins 7/8/12/13 are its signal input terminals and pins 3/1 are their signal output terminals; for LM1875, it has totally 5 pins, being a high-performance single-channel power amplifier IC. The applied circuit is very simple and has a 15W power output in rated status. Pin 5 and pin 3 are positive and negative power supply pins. $\pm 22V$ power supply is used in this device. Pin 1 is signal input terminal, pin 2 is feedback input terminal and pin 4 is output terminal.

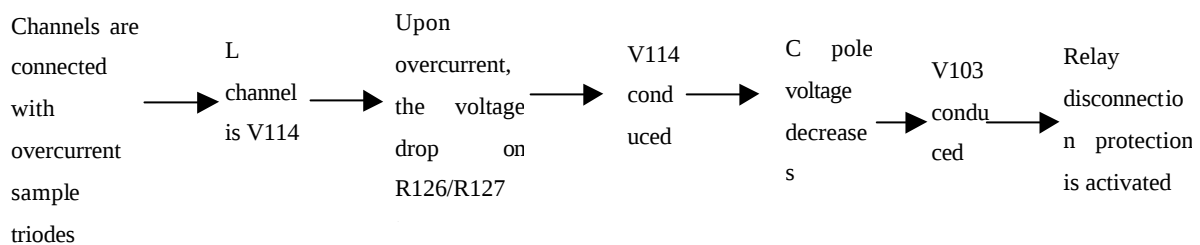
III. Protection circuit: The way of protection for L/R channel is to disconnect relay Y100, and meanwhile, CPU sends P_LRM mute signal to mute main channel to disable output. For C/SR/SL channel, CPU sends MUTE (P_CSM) signal (high level) to mute two “surround channels” and “center channel”. Their control terminals are connected to disable outputs of five channels upon startup. AV100 has the following ways of protection:

1. Startup delay closing protection circuit: Since that the circuit is unstable upon startup and the impact current produced greatly harms the sound box and power amplifier circuit, so delay closing protection circuit is provided. Upon startup, +22V charges up C115 via R108, and the positive voltage of C115 rises gradually. When it exceeds 5.1V, VD411 is inversely struck through, and its positive pole outputs high level to add to the base electrodes of the compound tube made up of V105 and V104. Now the compound tube is conduced, relay Y100 closes and the device has normal output. The startup delay closing time depends on the charging and discharging time constant. Its working process is as follows: +22V charges up C115 via R108 and strikes through down VD111 inversely, so as to conduce V105/V104 positively and finally close relay Y100. Left, right and central channels conduct startup impact protection in the following way: When the system is reset, CPU's pin 33 outputs a high level, which goes through R164 and pin 9/14 of LM4731 to make LM4731 to output mute. After the successful delayed startup of device and normal closing of the delay, the level of CPU's pin 33 is reduced and shifted to low level, so that LM4731 begins to enter normal working status and SL/SR channel outputs normally.

2. Central point overvoltage protection: An overvoltage sampling resistance is connected to the output terminal of each channel. L channel is R116. When the output central point of a channel has a DC voltage greater than +3.5V or lower than -3.5V, V101 or V102 is conduced, reducing their C pole voltage. V103 is then conduced and finally the relay is disconnected to protect circuit startup; now pin 8 of the relay returns a high level P_Rly to CPU's pin 33. Immediately CPU's pin 35/36 sends high level to main channel and central surround channel to mute channels; meanwhile, CPU's pin 34 P_RC sends high level and positively conduces V100 (9014), so as to lower the base voltage of V103 and the failure state is delayed and maintained. After about 5 seconds, CPU's pin 34 P_RC shifts to low level and the power supply begins to charge up C115. If troubleshooting is successful,

when C115 is charged up to about 5.5V, the relay will close again; if troubleshooting is failed, after three times of system testing, the device will enter into complete protection state; now all buttons are disabled and functional operation is only available when the device is restarted and troubleshooting is done.

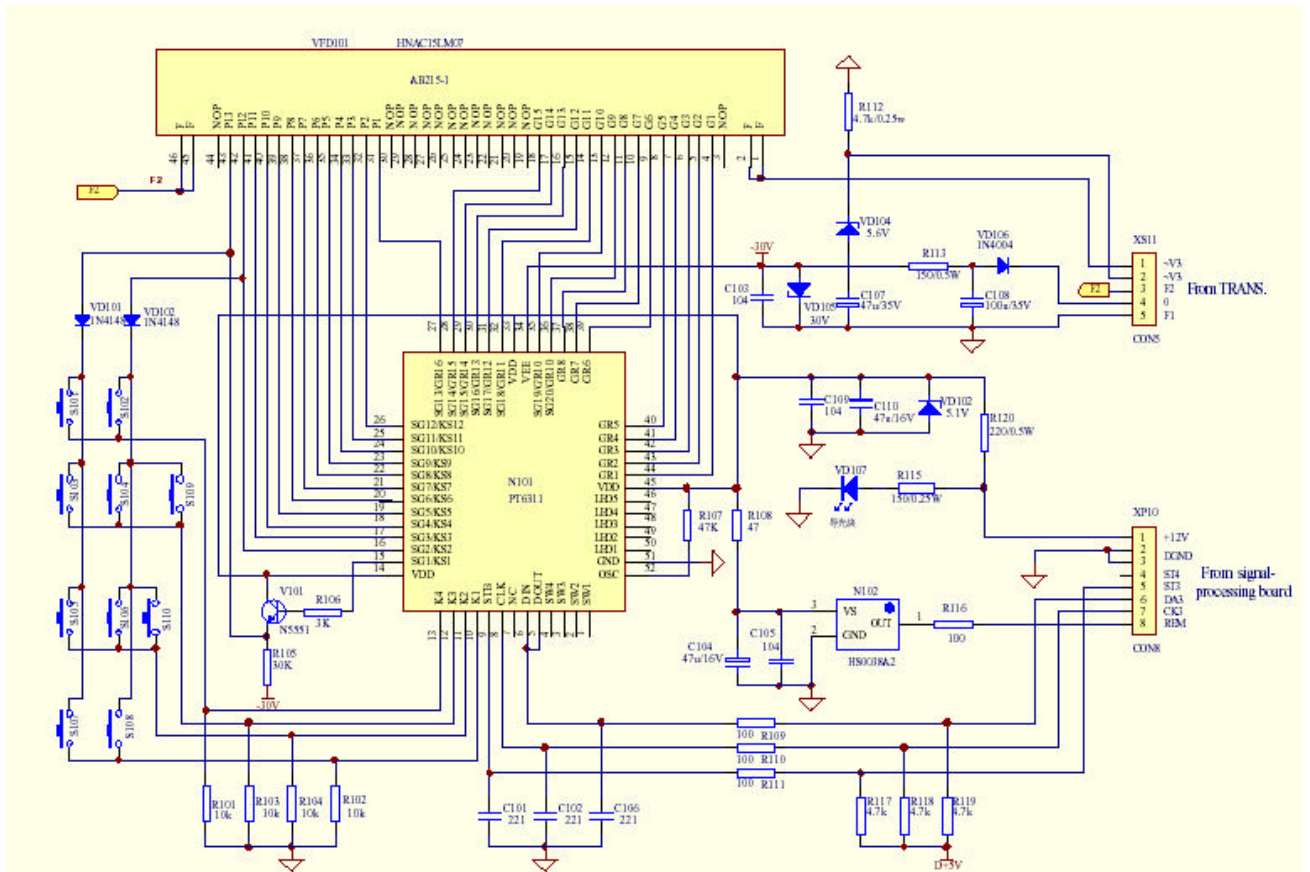
3. Over-current and short circuit protection: An over-current sampling triode is connected in parallel on each of the output load resistances of L/R channels. Other three channels (SL/SR/C) are provided with over-current protection in the power amplifier IC. When one of L/R channels is subject to over-current failure, the voltage drop produced on R126 and R127 will increase rapidly. Once the voltage drop produced on R129 exceeds 0.7V, V426 will be conducted. V103 is then conducted and finally the relay is disconnected to protect circuit startup; now pin 8 of the relay returns a high level P_Rly to CPU's pin 33. Immediately CPU's pin 35/36 sends high level to main channel and central surround channel to mute channels; meanwhile, CPU's pin 34 P_RC sends high level and positively conduces V100 (9014), so as to lower the base voltage of V103 and the failure state is delayed and maintained. After about 5 seconds, CPU's pin 34 P_RC shifts to low level and the power supply begins to charge up C115. If troubleshooting is successful, when C115 is charged up to about 5.5V, the relay will close again; if troubleshooting fails, after three times of system testing, the device will enter into complete protection state; now all buttons are disabled and functional operation is only available when the device is restarted and troubleshooting is done.



III. Description of Circuits

1. Control panel

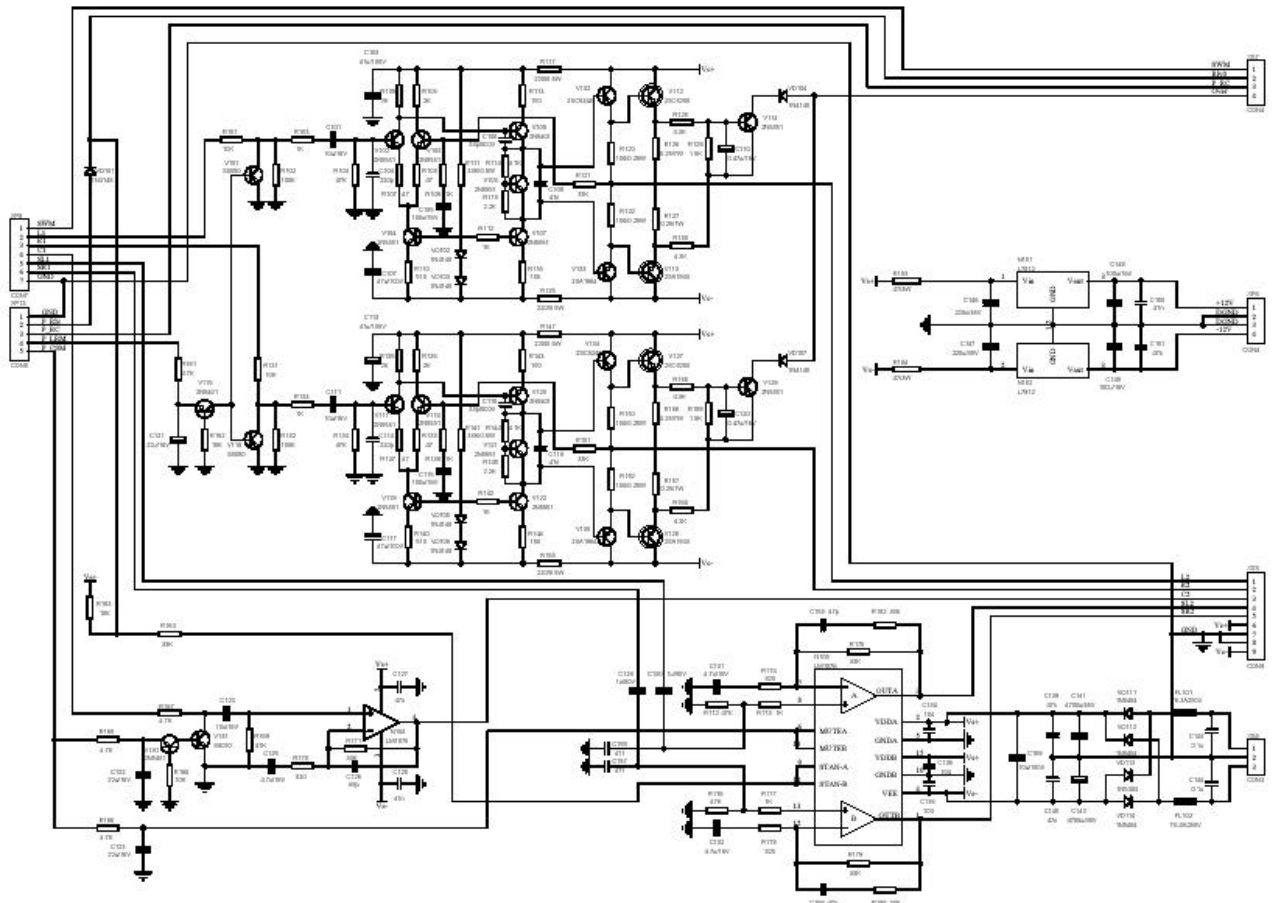
- Attachments: AV100 (RU) parts list —control panel
Control panel schematic diagram .SCH



2. Main power amplifier board

Main parts list

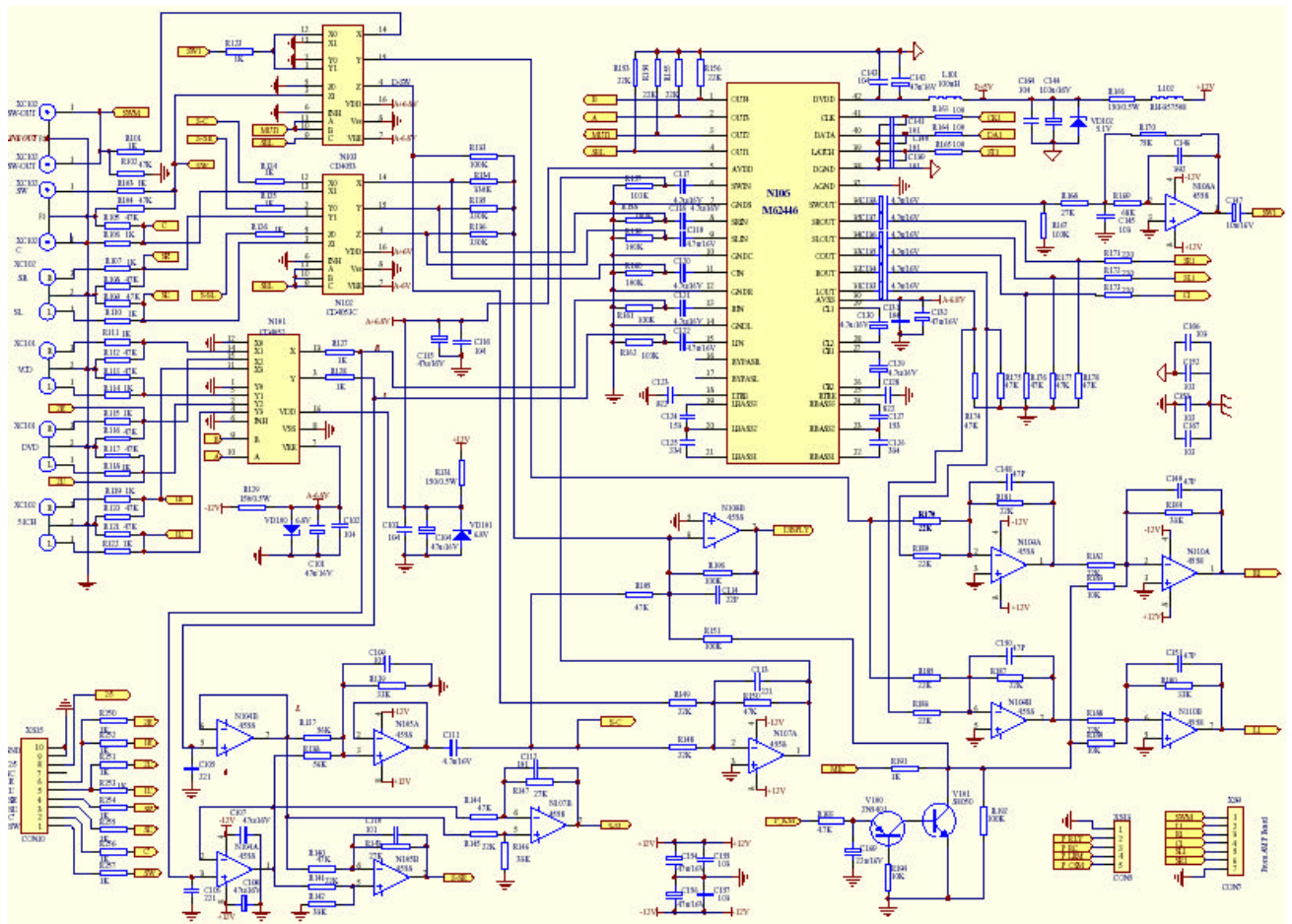
- Attachments: AV100 (RU) parts list —main power amplifier board
- Power amplifier board. SCH



3.Signal processing board

Main parts list

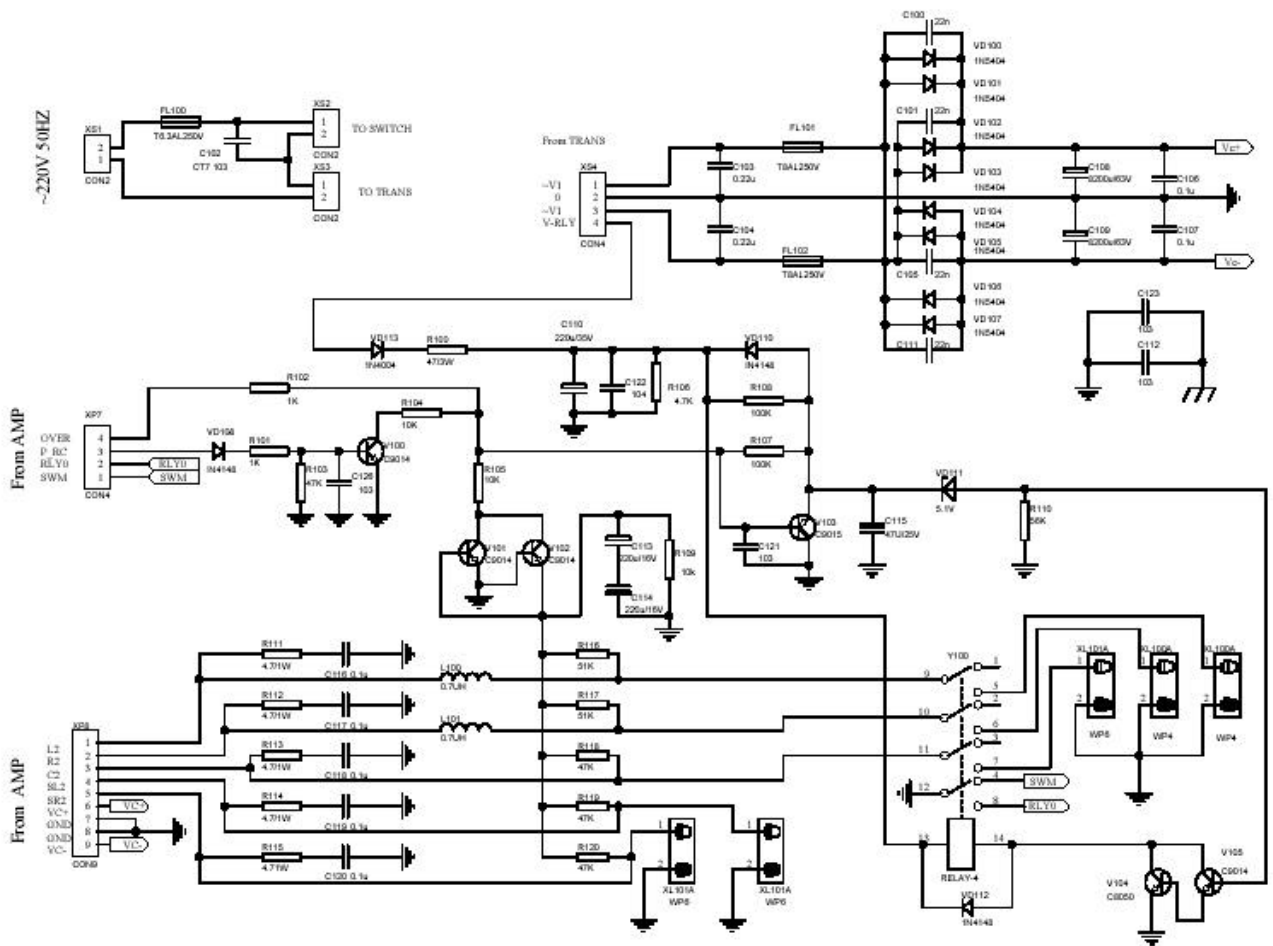
- Attachments: AV100 (RU) parts list—signal processing board
Signal processing board. SCH



4. Power panel

Main parts list

- Attachments: AV100 (RU) parts list—power panel
Power board. SCH



5. CPU board

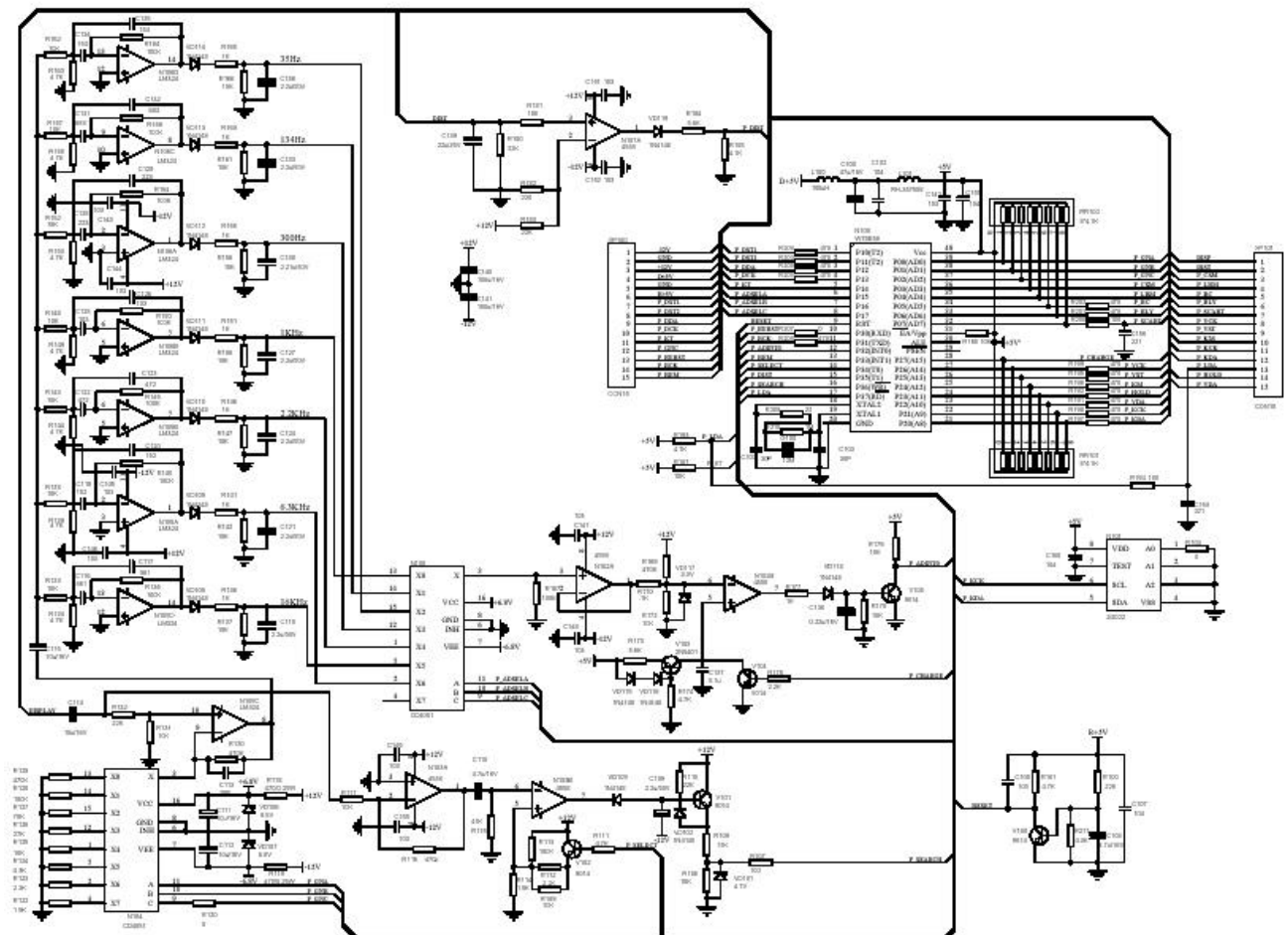
Main parts list

- Attachments: AV100 (RU) parts list—CPU board

CPU

board.

SCH



V. Description of Important ICs and Pin Functions

- N100 SM8958A 8-digit microprocessor, overall control CPU, for device functional control (CPU board)
Attachment: IC SM8958A.pdf
- N101 24C02 status register, for saving working statuses before shutdown and memory function (CPU board)
Attachment: IC 24C02.pdf
- N106 M62446 6-channel electronic volume control (signal processing board)
Attachment: IC M62446.pdf
- N113 PT2399 reverberation processing IC (signal processing board)
Attachment: IC PT2399.pdf
- N105 LM4731 integrated power IC, surround channel power amplifier (power amplifier board)
Attachment: IC LM4731.pdf
- N101 SC0791 panel drive IC (PT16311 compatible) (control panel)
Attachment: IC SC0791.pdf